CLAIM AMENDMENTS:

Claim 1 (Previously Presented): A semiconductor device, comprising:

a semiconductor substrate; and

a fuse circuit disposed on the semiconductor substrate, and which comprises a first conductive region and a second conductive region,

wherein the first conductive region has a multi-layered structure, and the second conductive region has a less layered structure than the first conductive region;

wherein the first conductive region include a plurality of conductive layers, and a respective interlayer insulating layer disposed between respective adjacent ones of the conductive layers; and

wherein said fuse circuit comprises first and second electrode pads, and a conductive line extending from said first electrode pad to said second electrode pad, said first conductive region and said second conductive region collectively forming said conductive line, and being disposed between said first and second electrode pads.

Claim 2 (Original): A semiconductor device according to claim 1, wherein the second conductive region is formed to have a single layer structure.

Claim 3 (Currently Amended): A semiconductor device ~~according to claim 2~~, comprising:

a semiconductor substrate; and

a fuse circuit disposed on the semiconductor substrate, and which comprises a first conductive region and a second conductive region,

wherein the first conductive region has a multi-layered structure, and the second conductive region has a less layered structure than the first conductive region;

wherein the first conductive region include a plurality of conductive layers, and a respective interlayer insulating layer disposed between respective adjacent ones of the conductive layers; and

wherein said fuse circuit comprises first and second electrode pads, and a conductive line extending from said first electrode pad to said second electrode pad, said first conductive region and said second conductive region collectively forming said conductive line, and being disposed between said first and second electrode pads;

wherein the second conductive region is formed to have a single layer structure; and

wherein the second conductive region is formed as an upper most layer.

Claim 4 (Original): A semiconductor device according to claim 3, wherein no passivation layer is formed over the second conductive region.

Claim 5 (Original): A semiconductor device according to claim 1, comprising:

a plurality of the fuse circuits, which are arranged so that the second conductive regions are not located adjacent one another.

Claim 6 (Currently Amended): A semiconductor device ~~according to claim 1~~, comprising:

a semiconductor substrate; and

a fuse circuit disposed on the semiconductor substrate, and which comprises a first conductive region and a second conductive region,

wherein the first conductive region has a multi-layered structure, and the second conductive region has a less layered structure than the first conductive region;

wherein the first conductive region include a plurality of conductive layers, and a respective interlayer insulating layer disposed between respective adjacent ones of the conductive layers;

wherein said fuse circuit comprises first and second electrode pads, and a conductive line extending from said first electrode pad to said second electrode pad, said first conductive region and said second conductive region collectively forming said conductive line, and being disposed between said first and second electrode pads; and

wherein a length of the second conductive region along the conductive line is formed not to be larger than a double of a width of the conductive line.

Claim 7 (Original): A semiconductor device according to claim 1, wherein the fuse circuit is provided with through holes in the first conductive region to connect the layers to each other.

Claim 8 (Previously Presented): A semiconductor device according to claim 7, wherein a predetermined voltage is applied between the first and second electrode pads in order to disconnect the second conductive region.

Claim 9 (Original): A semiconductor device according to claim 1, wherein a laser beam is applied to the second conductive region in order to disconnect it.

Claim 10 (Original): A semiconductor device according to claim 1, wherein the fuse circuit is applicable to one selected from a redundant fuse in a semiconductor device; a fuse adjusting a resistance and/or capacity in a semiconductor device; a fuse used for switching logic circuits in a semiconductor device; and a fuse used for adjusting an output level of signal in a semiconductor device.

Claims 11-20 (canceled).

Claim 21 (Previously Presented): A semiconductor device according to claim 1, wherein the first conductive region and the second conductive region form a bridge structure, with the second conductive region extending over the semiconductor substrate with a space therebetween.

Claim 22 (Previously Presented): A semiconductor device according to claim 21, wherein the second conductive region forms an uppermost layer.

Claim 23 (Currently Amended): A semiconductor device according ~~to claim 1~~, comprising:

a semiconductor substrate; and

a fuse circuit disposed on the semiconductor substrate, and which comprises a first conductive region and a second conductive region,

wherein the first conductive region has a multi-layered structure, and the second conductive region has a less layered structure than the first conductive region;

wherein the first conductive region include a plurality of conductive layers, and a respective interlayer insulating layer disposed between respective adjacent ones of the conductive layers;

wherein said fuse circuit comprises first and second electrode pads, and a conductive line extending from said first electrode pad to said second electrode

pad, said first conductive region and said second conductive region collectively forming said conductive line, and being disposed between said first and second electrode pads; and

wherein the first conductive region and the second conductive region form a bridge structure, with the second conductive region being an upper layer that is suspended over the semiconductor substrate.

Claim 24 (Previously Presented): A semiconductor device according to claim 23, wherein the second conductive region forms an uppermost layer.

Claim 25 (Previously Presented): A semiconductor device according to claim 1, wherein a lower surface of the second conductive region is disposed directly over and immediately adjacent to a space.

Claim 26 (Canceled).

Claim 27 (Previously Presented): A semiconductor device according to claim 1, wherein electric current flows from said first conductive pad, through the conductive line, and to said second conductive pad, respectively, and wherein when the electric current exceeds a threshold level, the conductive line melts, to prevent the flow of the electric current.